

CLAIMS

What is claimed is:

- 1 1. A method, comprising:
2 receiving a selection signal;
3 receiving an erase-mode signal;
4 determining a level-shifter signal from the selection signal and the erase-
5 mode signal;
6 determining an inverter signal from the level-shifter signal and the
7 selection signal;
8 outputting the erase-mode signal in response to a first combination of the
9 inverter signal and the level-shifter signal; and
10 outputting a read-mode signal in response to a second combination of the
11 inverter signal and the level-shifter signal.
- 1 2. The method of claim 1, ~~further~~ comprising:
2 receiving a non-erase-mode signal; and
3 outputting the read-mode signal.
- 1 3. The method of claim 2, wherein outputting the read-mode signal comprises
2 supplying a low impedance, low voltage current.
- 1 4. The method of claim 1, wherein said receiving a selection signal comprises
2 combining a first signal and a second signal with a nand operation.
- 1 5. The method of claim 1, wherein said receiving an erase-mode signal comprises
2 receiving an erase-mode signal having a negative voltage.
- 1 6. The method of claim 1, wherein said determining a level-shifter signal from the
2 selection signal and the erase-mode signal comprises pulling up a voltage from a
3 negative erase-mode voltage.

1 7. The method of claim 1, wherein said determining an inverter signal from the
2 level-shifter signal and the selection signal comprises choosing between the level-
3 shifter signal and the selection signal.

1 8. The method of claim 1, wherein said outputting the erase-mode signal in response
2 to a first combination of the inverter signal and the level-shifter signal comprises
3 outputting a negative erase-mode voltage in response to a positive voltage inverter
4 signal and a negative voltage level-shifter signal.

1 9. The method of claim 1, wherein said outputting a read-mode signal in response to
2 a second combination of the inverter signal and the level-shifter signal comprises
3 outputting the read-mode signal in response to a negative voltage inverter signal
4 and a negative voltage level-shifter signal.

1 10. An apparatus, comprising:
2 a level shift stage circuit coupled to a selection signal input and coupled a
3 negative charge pump input;
4 an invert stage circuit coupled to said level shift stage circuit and
5 responsively coupled to the selection signal input; and
6 an output stage circuit coupled to said invert stage circuit to switch an
7 output between a read-mode signal and an erase-mode signal
8 dependent upon the selection signal input.

1 11. The apparatus of claim 10, wherein said level shift stage circuit comprises:
2 a current source pull-down circuit; and
3 an active source pull-up circuit coupled to the current source pull-down
4 circuit.

1 12. The apparatus of claim 11, wherein the current source pull-down circuit
2 comprises:
3 a first transistor having a gate coupled to a bias input and a source/drain
4 coupled to a negative charge pump input; and
5 a first cascode transistor having a source/drain coupled a drain/source of
6 the first transistor, and a gate coupled to a cascode input.

1 13. The apparatus of claim 11, wherein the active source pull-up circuit comprises:
2 a second transistor having a source/drain coupled to a pull-up input and a
3 gate coupled to the selection signal input; and
4 a second cascode transistor having a source/drain coupled to a drain/source
5 of the second transistor, a drain/source coupled to the current
6 source pull-down circuit, and a gate coupled to a cascode input.

1 14. The apparatus of claim 11, wherein the current pull-down circuit comprises a
2 triple-well, n-channel, insulated gate transistor.

- 1 15. The apparatus of claim 11, wherein the active pull-up circuit comprises a p-
2 channel transistor.
- 1 16. The apparatus of claim 10, wherein said invert stage circuit comprises:
2 an invert-to-read-mode-signal circuit; and
3 an invert-to-erase-mode-signal circuit coupled to the invert-to-read-mode-
4 signal circuit.
- 1 17. The apparatus of claim 16, wherein the invert-to-read-mode-signal circuit
2 comprises:
3 a third transistor having a source/drain coupled to the selection signal input
4 and a gate coupled to a circuit ground; and
5 a third cascode transistor having a source/drain coupled to a drain/source
6 of the third transistor, a drain/source coupled to the invert-to-erase-
7 mode-signal circuit, and a gate coupled to the cascode input.
- 1 18. The apparatus of claim 16, wherein the invert-to-erase-mode-signal circuit
2 comprises:
3 a fourth transistor having a source/drain coupled to the negative charge
4 pump input and a gate coupled to said level shift stage circuit; and
5 a fourth cascode transistor having a source/drain coupled to a drain/source
6 of the fourth transistor, a drain/source coupled to the drain/source
7 of the third cascode transistor, and a gate coupled to the cascode
8 input.
- 1 19. The apparatus of claim 10, wherein said output stage circuit comprises:
2 an output-read-mode-signal circuit coupled to an output; and
3 an output-erase-mode-signal circuit coupled to the output.
- 1 20. The apparatus of claim 19, wherein the output-read-mode-signal circuit comprises
2 a fifth transistor having a source/drain coupled to the circuit ground, a gate
3 coupled to said invert stage circuit, and a drain/source coupled to the output.

1 21. The apparatus of claim 20, wherein the fifth transistor comprises a low resistance
2 channel.

1 22. The apparatus of claim 19, wherein the output-erase-mode-signal circuit
2 comprises:

3 a sixth transistor having a source/drain coupled to the negative charge
4 pump input, and a gate coupled to said invert stage circuit; and
5 a sixth cascode transistor having a source/drain coupled to a drain/source
6 of the sixth transistor, a gate coupled to a cascode input, and a
7 drain/source coupled to the output.

1 23. The apparatus of claim 10, wherein said level shift stage circuit comprises a
2 transistor having a ringed drain/source.

1 24. The apparatus of claim 10, wherein the erase-mode signal comprises a high
2 magnitude negative voltage.

1 25. A system, comprising:
2 a memory array; and
3 a memory array controller comprising
4 a negative charge pump; and
5 a block controller coupled to the negative charge pump,
6 comprising:
7 a negative level shifter to switch an output between a read-
8 mode voltage and an erase-mode voltage dependent
9 upon a selection signal input;
10 a positive voltage switch coupled to the negative level shift
11 circuit;
12 a bit line driver coupled to the positive switch and coupled
13 to said memory array; and
14 a word line driver coupled to said positive switch, coupled
15 to the negative level shifter, and coupled to said
16 memory array.

1 26. The system of claim 25, wherein the negative level shifter comprises an output
2 stage comprising an n-channel transistor.

1 27. The system of claim 25, wherein the negative level shifter comprises an active
2 pull-up circuit coupled to a current source pull-down circuit.

1 28. The system of claim 25, wherein the erase-mode voltage comprises a high
2 magnitude negative voltage.

1 29. The system of claim 25, wherein the read-mode voltage comprises a low voltage
2 current from the negative charge pump via a low resistance n-channel transistor.

1 30. The system of claim 25, wherein said memory array comprises a block coupled to
2 the block controller and having a bit line, a word line, and a source line.

1 31. The system of claim 25, wherein said memory array controller comprises the block
2 controller to apply a signal to a first block within said memory array to erase the first
3 block.

1 32. The system of claim 25, wherein said memory array controller comprises a second
2 block controller to apply a signal to a second block within said memory array to read a
3 memory cell of the second block substantially simultaneously with erasure of a first
4 block within said memory array.

1 33. The system of claim 25, wherein the negative charge pump comprises an output circuit
2 to output the erase-mode voltage.

1 34. The system of claim 25, wherein the negative level shifter comprises an output stage
2 circuit coupled to said memory array to apply the erase-mode voltage to a source line
3 of said memory array.

1 35. The system of claim 34, wherein the output stage circuit comprises a transistor to
2 couple the output of the negative charge pump to the source line.

1 36. The system of claim 25, wherein the negative level shifter comprises a first circuit to
2 pull up an output of the negative charge pump to apply a read-mode voltage to a first
3 memory cell of said memory array.

1 37. The system of claim 36, further comprising a second negative level shifter coupled to
2 the negative charge pump to couple the output of the negative charge pump to a second
3 memory cell of said memory array substantially simultaneously with the application of
4 the read-mode voltage to the first memory cell of said memory array.

1 38. The system of claim 36, wherein the first circuit comprises circuitry to substantially
2 prevent current burn within the negative level shifter.

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39. The system of claim 36, wherein the first circuit comprises an output stage circuit to apply a low resistance current to the first memory cell.

1 40. A method, comprising:
2 receiving a signal to erase a first block within a memory array;
3 lowering an output of a negative charge pump to a negative voltage;
4 applying the output of the negative charge pump to a source line of the first
5 block; and
6 pulling up the output of the negative charge pump to apply a read-mode voltage
7 to a memory cell of a second block within the memory array
8 substantially simultaneously with said applying the output.

1 41. The method of claim 40, further comprising applying a signal to a word line and a bit
2 line to erase the first block.

1 42. The method of claim 40, further comprising applying a signal to a word line and a bit
2 line of the second block to ~~read~~ the memory cell substantially simultaneously with
3 erasing the first block.

1 43. The method of claim 40, wherein said receiving a signal to erase a first block within a
2 memory array comprises:
3 receiving an instruction to erase the first block; and
4 receiving an instruction to read the memory cell prior to erasure of the first
5 block.

1 44. The method of claim 40, wherein said lowering an output of a negative charge pump to
2 a negative voltage comprises lowering the output of the negative charge pump to a
3 high magnitude, negative voltage.

1 45. The method of claim 40, wherein said applying the output of the negative charge pump
2 to a source line of the first block comprises coupling the output of the negative charge
3 pump to the source line.

1 46. The method of claim 40, wherein said pulling up the output comprises turning off
2 transistors to substantially prevent current burn within a negative level shifter coupled
3 to the second block of memory.

1 47. The method of claim 40, wherein said pulling up the output comprises applying a low
2 resistance current to the memory cell.

1 48. An apparatus, comprising:
2 a negative charge pump; and
3 a block controller coupled to the negative charge pump, comprising:
4 a negative level shifter to switch an output between a read-mode
5 voltage and an erase-mode voltage dependent upon a selection
6 signal input; and
7 a positive voltage switch coupled to the negative level shifter.

1 49. The apparatus of claim 48, wherein the negative level shifter comprises an output stage
2 circuit to couple to said negative charge pump to output the erase-mode voltage.

1 50. The apparatus of claim 48, wherein the negative level shifter comprises a first circuit
2 to pull up an output of said negative charge pump to output a read-mode voltage.

1 51. The apparatus of claim 50, further comprising a second negative level shifter to couple
2 to said negative charge pump to output an erase-mode voltage substantially
3 simultaneously with an output of the read-mode voltage by the negative level shifter.